ESP32 RMT Register Summary

Name	Description	Address	Access	reset value
RMT base address	RMT base address	0x3FF56000		
	end	0x3FF56FFF		
	The R/W ram address for channel0 by apb fifo access	0x3ff56000		0
		0x3ff56004		0
		0x3ff56008		0
		0x3ff5600C		0
		0x3ff56010		0
		0x3ff56014		0
		0x3ff56018		0
	The R/W ram address for channel7 by apb fifo access	0x3ff5601C		0
Configuration registers				
RMT_CH0CONF0_REG	Channel 0 config register 0	0x3FF56020	R/W	0x31100002
RMT_CH0CONF1_REG	Channel 0 config register 1	0x3FF56024	R/W	0x00000F20
RMT_CH1CONF0_REG	Channel 1 config register 0	0x3FF56028	R/W	0x31100002
RMT_CH1CONF1_REG	Channel 1 config register 1	0x3FF5602C	R/W	0x00000F20
RMT_CH2CONF0_REG	Channel 2 config register 0	0x3FF56030	R/W	0x31100002
RMT_CH2CONF1_REG	Channel 2 config register 1	0x3FF56034	R/W	0x00000F20
RMT_CH3CONF0_REG	Channel 3 config register 0	0x3FF56038	R/W	0x31100002
RMT_CH3CONF1_REG	Channel 3 config register 1	0x3FF5603C	R/W	0x00000F20
RMT_CH4CONF0_REG	Channel 4 config register 0	0x3FF56040	R/W	0x31100002
RMT_CH4CONF1_REG	Channel 4 config register 1	0x3FF56044	R/W	0x00000F20
RMT_CH5CONF0_REG	Channel 5 config register 0	0x3FF56048	R/W	0x31100002
RMT_CH5CONF1_REG	Channel 5 config register 1	0x3FF5604C	R/W	0x00000F20
RMT_CH6CONF0_REG	Channel 6 config register 0	0x3FF56050	R/W	0x31100002
RMT_CH6CONF1_REG	Channel 6 config register 1	0x3FF56054	R/W	0x00000F20
RMT_CH7CONF0_REG	Channel 7 config register 0	0x3FF56058	R/W	0x31100002
RMT_CH7CONF1_REG	Channel 7 config register 1	0x3FF5605C	R/W	0x00000F20
RMT_CH0STATUS_REG		0x3FF56060		0
RMT_CH1STATUS_REG		0x3FF56064		0x040040
RMT_CH2STATUS_REG		0x3FF56068		0x080080
RMT_CH3STATUS_REG		0x3FF5606C		0x0C00C0
RMT_CH4STATUS_REG		0x3FF56070		0x100100
RMT_CH5STATUS_REG		0x3FF56074		0x140140
RMT_CH6STATUS_REG		0x3FF56078		0x180180
RMT_CH7STATUS_REG		0x3FF5607C		0x1C01C0
RMT_CH0ADDR_REG	The ram relative address in channel0 by apb fifo access	0x3FF56080		0
RMT_CH1ADDR_REG		0x3FF56084		0x040040
RMT_CH2ADDR_REG		0x3FF56088		0x080080
RMT_CH3ADDR_REG		0x3FF5608C		0x0C00C0
RMT_CH4ADDR_REG		0x3FF56090		0x100100
RMT_CH5ADDR_REG		0x3FF56094		0x140140
RMT_CH6ADDR_REG		0x3FF56098		0x180180
RMT_CH7ADDR_REG	The ram relative address in channel7 by apb fifo access	0x3FF5609C		0x1C01C0
Interrupt registers				
RMT_INT_RAW_REG	Raw interrupt status	0x3FF560A0	RO	0
RMT_INT_ST_REG	Masked interrupt status	0x3FF560A4	RO	0
RMT_INT_ENA_REG	Interrupt enable bits	0x3FF560A8	R/W	0
RMT_INT_CLR_REG	Interrupt clear bits	0x3FF560AC	WO	0
Carrier wave duty cycle registers				
RMT_CH0CARRIER_DUTY_REG	Channel 0 duty cycle configuration register	0x3FF560B0	R/W	0x400040
RMT_CH1CARRIER_DUTY_REG	Channel 1 duty cycle configuration register	0x3FF560B4	R/W	0x400040

RMT_CH2CARRIER_DUTY_REG	Channel 2 duty cycle configuration register	0x3FF560B8	R/W	0x400040
RMT_CH3CARRIER_DUTY_REG	Channel 3 duty cycle configuration register	0x3FF560BC	R/W	0x400040
RMT_CH4CARRIER_DUTY_REG	Channel 4 duty cycle configuration register	0x3FF560C0	R/W	0x400040
RMT_CH5CARRIER_DUTY_REG	Channel 5 duty cycle configuration register	0x3FF560C4	R/W	0x400040
RMT_CH6CARRIER_DUTY_REG	Channel 6 duty cycle configuration register	0x3FF560C8	R/W	0x400040
RMT_CH7CARRIER_DUTY_REG	Channel 7 duty cycle configuration register	0x3FF560CC	R/W	0x400040
Tx event configuration registers				
RMT_CH0_TX_LIM_REG	Channel 0 Tx event configuration register	0x3FF560D0	R/W	0x80
RMT_CH1_TX_LIM_REG	Channel 1 Tx event configuration register	0x3FF560D4	R/W	0x80
RMT_CH2_TX_LIM_REG	Channel 2 Tx event configuration register	0x3FF560D8	R/W	0x80
RMT_CH3_TX_LIM_REG	Channel 3 Tx event configuration register	0x3FF560DC	R/W	0x80
RMT_CH4_TX_LIM_REG	Channel 4 Tx event configuration register	0x3FF560E0	R/W	0x80
RMT_CH5_TX_LIM_REG	Channel 5 Tx event configuration register	0x3FF560E4	R/W	0x80
RMT_CH6_TX_LIM_REG	Channel 6 Tx event configuration register	0x3FF560E8	R/W	0x80
RMT_CH7_TX_LIM_REG	Channel 7 Tx event configuration register	0x3FF560EC	R/W	0x80
Other registers				
RMT_APB_CONF_REG	RMT-wide configuration register	0x3FF560F0	R/W	0
?	reserved	0x3FF560F4		0
?	reserved	0x3FF560F8		0
RMT_DATE_REG	version register	0x3FF560FC		0x16022600
	0x3FF56100 - 0x3FF561FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56200 - 0x3FF562FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56300 - 0x3FF563FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56400 - 0x3FF564FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56500 - 0x3FF565FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56600 - 0x3FF566FF = 0x3FF56000 - 0x3FF560FF			
	0x3FF56700 - 0x3FF567FF = 0x3FF56000 - 0x3FF560FF			
	chanel 0 memory start	0x3FF56800	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
	chanel 0 memory end	0x3FF568FF	R/W	undefined
		0x3FF56900	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF569FF	R/W	undefined
		0x3FF56A00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF56AFF	R/W	undefined
		0x3FF56B00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF56BFF	R/W	undefined
		0x3FF56C00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF56CFF	R/W	undefined
		0x3FF56D00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF56DFF	R/W	undefined
		0x3FF56E00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
		0x3FF56EFF	R/W	undefined

	chanel 7 memory start	0x3FF56F00	R/W	undefined
		.	R/W	undefined
		.	R/W	undefined
	chanel 7 memory end	0x3FF56FFF	R/W	undefined

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